



IP Workflow Development with ST2110 and VC2 Compression

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IP SHOWCASE THEATRE AT IBC2019 : 13-17 SEPT 2019



IP Workflow Testbed Design with ST2110 & VC2

- 1. Introduction to the Testbed
- 2. SDI-ST2110 Converter
- 3. VC2 Codec for IP Workflow
- 4. Audio over IP (treated as Ancillary data)
- 5. Discussion

TECHNOLOGY INTO REALITY Interactive Media Lab



- Where is the Testbed studio ?
 - KBS Laboratory Building, IP Workflow Testbed (Panoramic view)



– Miniature Studio







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ST2110 & VC2 : Introduction

- Who built the workflow ? (Consortium Organization)
 - KBS (Korean Broadcasting System)
 - Architecture Developer, Testbed holder
 - ST2110-20/30 supporting media server developer

– Lumantek

- ST2110-20 supporting video switcher developer
- Web-based workflow manager developer









- Who built the workflow ? (Consortium Organization)
 - Atto-research
 - SDN OpenFlow switch & network structure developer



- IML
 - ST2110-22 VC-2(ST2042/2047) compression supporting SDI-IP converter developer
 - Stand-alone workflow manager developer



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ST2110 & VC2 : Introduction

- Why IP Workflow ?
 - Study New Technology
 - KBS is already operating an IP Studio with Grass Valley-Cisco solution
 - Test ST2110 interoperability with legacy UHD equipment
 - IP-enabled Video Switcher Development
 - Lumantek extends product line with IP capability
 - ST2110-20 supporting modular video switcher





- Why IP Workflow ?
 - UHD Video Compression for 10G Network
 - ST2042/2047 VC-2, the only open & released low latency codec
 - Long-distance source with limited communication bandwidth
 - Network Infrastructure
 - Broadcasting Company-wide IP network connectivity
 - All hardware & media assets are managed with IP connection



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ST2110 & VC2 : Introduction

- How to build ?
 - Use new IP standard
 - SMPTE ST2110 for media transport
 - AMWA NMOS for workflow management
 - Target Media
 - Video : UHD (3,840x2,160) @59.94p
 - Audio : only embedded 16ch audio is supported, yet to be extended to ST2110-30





• How to build ?

– Network

- 1G/10G/25G/40G/100G ethernet switches mixed in spine-leaf design
- Non-proprietary SDN(OpenFlow) with legacy IGMP support

- Video Coding

- ST2110-20 uncompressed and ST2110-22 compressed with VC2 co-existing design
- draft-ietf-payload-rtp-vc2hq-03 for VC2 transport



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ST2110 & VC2 : Introduction

- Control SystemImage: Co
- How to build ? (Components)



• How to build ? (Block design; Simplified)





ST2110 & VC2 : SDI-IP Converter





ST2110 & VC2 : SDI-IP Converter





ST2110 & VC2 : SDI-IP Converter

- What is developed ?
 - NMOS Manager
 - IS-04, IS-05 support
 - Built-in registration server
 - Connection control user interface







ST2110 & VC2 : VC2 Codec

VC2 Video Compression

- Input SDI
 - 12G-SDI 3,840x2,160 UHD 60p,59.94p, 50p
- Wavelet Slice & Filter
 - SMPTE ST2042-1-2017 slice 64x2 Luma Wavelet Slice
 - Legal53 filter (Haar0, Haar1)
- Compression Ratio
 - 4:1~10:1 Run-time Programmable,
 - slice to slice exact CBR for even video quality over a frame
- Latency
 - 200us for encoding & decoding & Buffering @(Legal53, 64x2 slice, slice CBR)
- Implementation
 - IML's own FPGA IP, https://www.xilinx.com/products/intellectual-property/1-puxmo7.html



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ST2110 & VC2 : VC2 Codec





ST2110 & VC2 : VC2 Codec

- Transmission of VC2-compressed Video
 - RTP packet structure
 - IETF draft-ietf-payload-rtp-vc2hq-03 is followed
 - Fixed number of compressed slices are packed in the payload \rightarrow RTP packet size varies
 - VC2 frame header packet is generated at each start of a frame
 → Compression ratio, filter type can be dynamically changed



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ST2110 & VC2 : VC2 Codec

- Transmission of VC2-compressed Video

 RTP packet sequence
 - Single Frame

 1st Packet
 2nd Packet

 Parse
 Sequence

 Information
 Header

 Encoded
 EOF

 Active Picture
 EOF





ST2110 & VC2 : VC2 Codec

- Transmission of VC2-compressed Video
 - Time Synchronization
 - No PTP timing information is used in encoder's RTP frame generation
 - Minimal latency from pixel input to RTP packet → No frame timing sync for RTP stream
 - Decoder generates video timing with input RTP packet data speed
 - Identification of Stream Type
 - SDP file "a=rtpmap:99 VC2/90000" for NMOS connecting managements
 - Detailed parameters in the first packet of a frame



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ST2110 & VC2 : VC2 Codec



– Phase Synchronized Transmission \rightarrow Multi-frame delay



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ST2110 & VC2 : Audio as ANC data

- Audio Over IP
 - Input SDI
 - 12G-SDI 16ch PCM audio
 - Transport
 - SMPTE ST2110-40 (NOT 30)
 - SMPTE ST272M, ST2082-10 Audio packet (16ch, 48kHz) treated as ANC data
 - Time Sync
 - The audio packet in SDI is regenerated in the original position in the SDI frame



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ST2110 & VC2 : Audio as ANC data

- Audio Over IP
 - Stream Management
 - Automatic port mapping with the video NMOS connection
 - Independent audio stream can also be generated
 - Usage
 - SDI audio embedded/de-embedded can be used





ST2110 & VC2 : Audio as ANC data

- Audio Over IP
 - Audio packets are regenerated in the original position
 - Possible from VC2 Encoding/Decoding delay





ST2110 & VC2 : Discussion

- What we got from the testbed
 - Interoperability of legacy(12G-SDI) equipment & ST2110 devices
 - Working fine
 - Unified management is required
 - IP-converter should "NMOS" for legacy equipment
 - Ethernet based configuration & management of legacy equipment may be used for generating NMOS data

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ST2110 & VC2 : Discussion

- What we got from the testbed
 - Timing Synchronization
 - All devices may not require PTP connection
 - Time synchronization is really done in contribution/distribution encoder
 - Frequency synchronization is required in video/audio creator
 - Video mixers should have frame buffer for mixed ST2110 WIDE, Gapped/Linear devices
 ← Phase synchronization
 - The other devices can follow the source timing with minimum latency



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ST2110 & VC2 : Discussion

- Future Works
 - Application of the Latest & New AMWA Standards
 - IS-04/05 update
 - IS-06/07/08/09/10 ...
 - Full-stack by VSF
 - VC2 Codec +
 - Add envelop coding in wavelet coefficients \rightarrow better PSNR
 - Better quantization factor guess algorithm for reduced logic size
 - Workflow Manager
 - Open source project for easily integrated IP workflow





For Further Discussion, Visit IML@2.A31

Thank you

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